Bridging the Infrastructure Gap Between Traditional Wire-Bond and TSV Semiconductor Package Technology

Wael Zohni

Vern Solberg, Belgacem Haba, Ph.D. and Ilyas Mohammed, Ph.D.
Invensas Corporation, San Jose, California USA
Interconnectology: Supply Chain Interconnect Shift

**Foundry Scaling**

- 45nm
- 32nm
- 28nm
- 22nm
- <22nm

**Packaging Scaling**

- 2.0mm
- 1.5mm
- 1.0mm
- 0.8mm
- <0.8mm

**Node Generation Package Size**

**Time**

**Cost/Chip**

Critical performance metrics are shifting from **CMOS scaling and package form factor** to **system level power consumption and bandwidth**.
Mobile Computing Trends

- Improved graphics (HD, 3D gaming)
- Increased functional density
- Multi-screen operation
- Extended battery life

* Source: Samsung, Apple, and EA Sports images
The Mobile Challenge

Denser: "Higher Capacity/mm³"

Cheaper: "Lower Power Use"

Faster: "Quicker Data Transfer"

2013

PoP

Bridge technology

2016?

3D-IC

Source: Samsung & Micron Images
Invensas Bridge Technology Platforms

**Bond-Via-Array (BVA™):**

-Provides high-bandwidth Package-on-Package (PoP) today using established wirebond assembly infrastructure
-Achieves over 1000 I/O density in existing 14mm standard PoP outline and height
-Smart to Verysmart phones
-Tablets & hybrid mobile devices

**Multi-Face-Down (xFD™):**

- High-performance multiple memory device package at lowered cost
- Dual-Face-Down (DFD) demonstrated in server RDIMM applications
- Quad (QFD) or “DIMM-in-a-Package” demonstrated in Ultrabook applications
- Also serves datacenters & cloud
Bond-Via-Array (BVA™)
PoP Broadly Used in Mobile Electronics

Source: UBM TechInsights (www.teardown.com)
Processor-Memory Stacking Solutions

- BVA offers the advantages of TSV (fine pitch and high number of interconnects) while utilizing existing packaging materials, processes and infrastructure.

<table>
<thead>
<tr>
<th></th>
<th>BGA</th>
<th>TMV</th>
<th>BVA</th>
<th>TSV (future)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pitch (mm)</td>
<td>0.5-0.65</td>
<td>0.4-0.5</td>
<td>0.2-0.4</td>
<td>0.05-0.2</td>
</tr>
<tr>
<td>IO</td>
<td>200-300</td>
<td>300-500</td>
<td>500-1500</td>
<td>1000+</td>
</tr>
</tbody>
</table>
BVA PoP Scalability

Assigning the same amount of area for IO as that of the current 0.5 mm pitch PoP, BVA with 0.2 mm pitch can offer up to 1464 IO.

Assumptions:
- Package size: 14 mm x 14 mm
- IO edge to package edge: \( \geq 0.4 \) mm
- IO area width: \( \leq 1 \) mm

<table>
<thead>
<tr>
<th>Pitch (mm)</th>
<th>No. of IO rows</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.50</td>
<td>200</td>
<td>288</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>0.40</td>
<td>256</td>
<td>372</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<tr>
<td>0.30</td>
<td>344</td>
<td>504</td>
<td>656</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>0.24</td>
<td>432</td>
<td>636</td>
<td>832</td>
<td>1020</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>0.20</td>
<td>520</td>
<td>768</td>
<td>1008</td>
<td>1240</td>
<td>1464</td>
<td></td>
</tr>
</tbody>
</table>
• 432 memory-logic interconnects were designed at 0.24 mm x 0.24 mm pitch to evaluate the feasibility of BVA technology.
1020 memory-logic interconnects were designed at 0.24 mm x 0.24 mm pitch to demonstrate the first wide IO PoP implementation.
BVA Interconnection: Free-standing Wires

- The nominal height of the wire-bonds is 0.5 mm.
BVA PoP Process Flow

- Conventional industry equipment and processes are used to assemble the BVA PoP
BVA Formation Utilizes Existing Wirebond Technology

- Demonstrated 240µm bond pitch with K&S Iconn wirebonder
- Vertical bond height, position and bond quality optimized during formation process
BVA Formation: Throughput

- Bond positional accuracy optimized with process development
- Bond cycle time is comparable to standard ball-stitch bonding
Molding and Tip Exposure: Process

Overmold height, exposed wire uniformity, wire cleanliness and wire tip quality optimized during process development.

Assembly Lab Yamada G-Line Mold Machine

Film Assist Mold

Overmold height, exposed wire uniformity, wire cleanliness and wire tip quality optimized during process development.
Molding and Tip Exposure: Cleaning

- Mechanical and chemical cleaning methods were tried to remove the mold residue from the wires.
- The results after plasma deflash are shown. The wires were clean.
PoP Stacking: Process

- The two packages are joined using conventional PoP SMT approach, with memory package solder balls reflowing around the wire tips.
- Two lots were processed by a third party assembler (Universal Instruments) with reported 100% stacking yield.
PoP Stacking: Results

• The package stack SMT yielded uniform and consistent joints at a very fine pitch of 0.24 mm.
## BVA PoP Reliability Test Results (432 IO TV)

<table>
<thead>
<tr>
<th>Test</th>
<th>Standard</th>
<th>Test condition</th>
<th>Sample size</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Moisture sensitivity Level 3</td>
<td>IPC/JEDEC-J-STD-020C</td>
<td>125°C for 24hrs; 30°C/60%RH for 192 hrs, 3X Pb-free reflow</td>
<td>22 logic and 22 memory packages</td>
<td>Pass</td>
</tr>
<tr>
<td>High temperature storage</td>
<td>JESD22-A103D-condition B</td>
<td>150°C, 1000 hours</td>
<td>22 PoP off-board</td>
<td>Pass</td>
</tr>
<tr>
<td>Unbiased autoclave</td>
<td>JESD22-A102D-condition D</td>
<td>121°C/100%RH/2atm for 168 hours</td>
<td>22 PoP off-board</td>
<td>Pass</td>
</tr>
<tr>
<td>Drop test</td>
<td>JESD22-B111</td>
<td>&gt;30 drops, 1500 G, 0.5 msec of half sine pulse</td>
<td>20 PoP on board with underfill</td>
<td>Pass (no failures till 128 drops)</td>
</tr>
<tr>
<td>Temperature cycling (board level)</td>
<td>JESD22-A104D Condition G</td>
<td>-40°C to 125°C, 1000 cycles</td>
<td>45 PoP on board with underfill</td>
<td>Pass</td>
</tr>
</tbody>
</table>

- 1020 IO TV reliability results due Q4’13
BVA PoP is a novel technology that realizes wide IO interface in conventional packaging.
Multi-Face-Down (xFD™) Package
Evolution of Single-Device DRAM Packaging

DIP

SOJ

TSOP

DRAM Device Layout (top view):

Centered Bond Pads

Single DRAM in TSOP (Cross-Section)

Wide-body Plastic Leadframe Wirebonded Package

CSP
TSOP to Window BGA Chip-Scale-Package (CSP)

- Entered production ~2000
- Current “De facto” standard for single-device DRAM packaging
- Reduced size (Chip-Scale)
- Higher performance

- Over 12 years of infrastructure development
- Established reliability
- Reduced material cost
  - Flex → BT
  - Film → Print Adhesive
  - SnPb → Pb-free
  - Increased volume
  - Short wirebonds

- Demonstrated High Volume Manufacturing
- More than 40 billion units shipped over last 6 years
- Infrastructure forms basis for xFD implementation
Invensas xFD™ Solution

Single Die DRAM Package
>Decade HVM, Billions of Units

DFD: Dual Face Down Package

Full Leverage of Established Assembly Infrastructure for High-Performance Multi-DRAM Package
Demonstrated xFD Variations

**Quad Die (QFD)**
(DIMM-in-a-Package)

- **Reduced size/cost:** xFD™ construction places multiple DRAM devices within an area similar to a traditional single-die component. Minimized materials and process steps result in reduced packaging cost per device.

- **Improved electrical performance:** Face-down wirebond configuration minimizes wirebond and overall electrical pathway length from device to package terminals. Furthermore, xFD™ pin-out arrangement extends design optimization advantages to module- and system board.

- **Improved thermal dissipation:** A stepped die stack arrangement that minimizes or eliminates need for spacer elements results in more rapid heat removal. Measurements have demonstrated 25% reduction in thermal resistance with xFD™ compared with conventional stacked DRAM packaging.

**Tri-Die (TFD)**

**Dual-Die (DFD)**
Comparison with Stacked DRAM Packages

Opposing-Face DDP
Long wires, unbalanced top/bottom signal length, thermal challenges

Face-Up DDP with FOW
Balanced signal length but at significant gold wire cost, difficult and cost Film-over-Wire material/process, thermals

Face-Up DDP with RDL
Balanced signal length, reduced gold wire but requires expensive re-distribution layer process, thermal challenges

Conventional structures: Two Passes Through Wirebond Line

Invensas: Single Pass through Wirebond Line (much less gold wire, no RDL) = lowest cost

Invensas Dual Face Down (DFD):
Two narrow slots are provided in the substrate to access the die bond pad pattern and accommodate the through-window wire-bond process.
Final phase of the package assembly includes an injection molding process, laser marking, ball attach, singulation, electrical test and burn-in.
Assembly Process Steps Comparison – QDPs vs DFD/QFD

**Invensas DFD/QFD**

1. Print 1st adhesive
2. Place 1st layer die + spacer
3. Dispense adhesive
4. Place 2nd layer die
5. 1-pass wirebond
6. Mold
7. Ball attach
8. Singulate

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**RDL QDP w/spacer**

1. RDL wafer**
2. Print 1st adhesive
3. Place 1st die
4. Wirebond 1st die
5. Dispense adhesive
6. Place spacer die
7. Dispense adhesive
8. Place 2nd die
9. Wirebond 2nd die
10. Dispense adhesive
11. Place spacer die
12. Dispense adhesive
13. Place 3rd die
14. Wirebond 3rd die
15. Dispense adhesive
16. Place spacer die
17. Dispense adhesive
18. Place 4th die
19. Wirebond 4th die
20. Mold
21. Ball attach
22. Singulate

**Wafer –Level RDL Process**

1. Dielectric Deposition
2. Mask, Etch Dielectric
3. Metal Deposition
4. Mask, Etch Metal
5. Dielectric Deposition
6. Mask, Etch Dielectric
7. NiAu plating

**DFD/QFD offers consolidated assembly process with reduced material use resulting in less cost**

22 steps

8 steps
Faster: Ultra-Short, Matched DIMM Breakout

- Efficient Address/Command breakout minimizes stub lengths & DIMM layer-count.
Ultrabook™ = Ultra-thin

NO VERTICAL SPACE TO ACCOMMODATE SODIMMs

→ Solder down memory is used on motherboard
Memory Footprint Shrink: Key to Improved Performance and Lower System Cost

**SO-DIMM vs QFD**

![Standard SO-DIMM](image)

80% space reduction when replacing SO-DIMM with Invensas QFD

**SDP vs DFD or QFD package options:**

- DFD
- QFD

Motherboard with onboard SDPs

Significant Size Reduction along with Reduced Package and System Cost
Denser: Thinner = Better Heat Transfer

Thin + 25% Heat Transfer Gain = 40% Cooling Cost Reduction in Data Center.
Component-level environmental test completed on functional DFD packages:
- Moisture pre-conditioning – JEDEC level III
- Highly-Accelerated-Stress-Test (HAST) – 240 hours
- Temperature Cycling – 1000 cycles

<table>
<thead>
<tr>
<th>Test</th>
<th>Quantity</th>
<th>Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level 3 Pre-conditioning (MSL3)</td>
<td>60 units</td>
<td>TC: -55°C/+125°C (5x) Baking: 125°C (12hours) Soaking: 30°C / 60%RH (192hours) Reflow: 3x 260°C</td>
<td>Pass</td>
</tr>
<tr>
<td>HAST</td>
<td>29* units</td>
<td>MSL3 + (Ta=+130°C; 85%Rh) 240 hours</td>
<td>Pass</td>
</tr>
<tr>
<td>Temperature Cycling</td>
<td>30 units</td>
<td>MSL3 + 1000 cycles -55°C/+125°C</td>
<td>Pass</td>
</tr>
</tbody>
</table>

* 1 unit removed due to handling damage
Summary: xFD Technology

- Brings single-device electrical performance to multi-DRAM packaging
- Verified high volume manufacturing process with existing equipment
- Less than half packaging cost of RDL-DDP
- About 25% improvement in thermal performance
- Design and performance advantages extend to module- and system-level
Thank You