DESIGN AND PROCESS OPTIMIZATION OF THROUGH SILICON VIA INTERPOSER FOR 3D-IC INTEGRATION

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ABSTRACT

The 3D-IC stacking technology provides improved performance, and reduced form factor for applications such as logic-memory integration, image sensors, MEMS, and LED. We present design and fabrication methods to implement Through Silicon Via (TSV) interposer. Cylindrical copper TSV’s of 20 µm diameter and 100 µm depth are fabricated in silicon. We present a method for design and process optimization, by recursive enhancement of parameters. Our approach includes selection of materials, proper thicknesses, tolerances, and geometries to achieve the specifications. A discussion on process module optimization and correlation among the whole will be given. We also present an analysis of the relative contribution to cost of each of the modules and identify areas for improvement.

Keywords: TSV, DRIE, CVD, interposer.

INTRODUCTION

For over 40 years CMOS scaling has been the driving force behind exponential growth in compute density and system level computing performance. However, the Moore’s Law paradigm is now undergoing unprecedented scrutiny as we face increasing cost pressures for the sub-22nm nodes and as memory bandwidth and latency become the limiting factors for most multi-core processors. In the past few years the silicon interposer has emerged as a potentially novel approach to extending computing performance without the high cost of CMOS scaling. The Interposer provides a flexible, high density wiring platform, from which component and system designers can explore the potential benefits of SOC partitioning, low latency Logic-Memory pairing, and full Logic partitioning among others.

The potential benefits of this approach have been widely discussed; however the industry adoption of this technology has been slowed by the significant complexity and cost of the Interposer and the required Through Silicon Via structures.

This paper provides a detailed analysis of silicon interposer design, parameter optimization, and fabrication. We also present the effect of different process modules on the interposer performance. We conclude with an analysis of the cost considerations of the current Interposer model flow and identify potential areas for future improvement.

TEST VEHICLE DESIGN

The interposer test vehicle is based on high density routings on topside, through-silicon vias (TSV) and low density routings on the backside of a 100 µm thick substrate, as shown in Figure 1. The vias have 40 µm copper pads with 45 µm pitch in the redistribution layer (RDL).

![Interposer geometry parameters](Figure 1)
About 2000 TSV’s in a daisy chain configuration link top and bottom routings for electrical testing. The oxide opening and TSV diameter is chosen to minimize process related defects such as lithography, maintain proper keep out area and via dummification is used to minimize stress accumulation. The key design parameters for the interposer test vehicle are summarized in Table 1. The die has a 10×10 mm footprint. Solder bumps have an inner pitch of 180 µm, a post-reflow diameter of 150 µm at a standoff height of 90 µm. The substrate will be thinned down to 100 µm to achieve TSV with aspect ratio of 5:1 for the 20 µm wide vias, providing adequate film coverage inside the via. Topside and backside copper will have a thickness of about 3 µm and polyimide (PI) thickness on both sides is about 5 to 6 µm. Topside side RDL utilizes 10 µm/10 µm Line/Space. The Under Bump Material (UBM) is self-aligned to copper pad at the top, but patterned and plated at the bottom side. Cadence Virtuoso was used to design the chip.

Table 1. Key Interposer Design parameters

<table>
<thead>
<tr>
<th>Part</th>
<th>Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(Si)</td>
<td>Silicon thickness</td>
</tr>
<tr>
<td>t(Sn)</td>
<td>Solder bump thickness</td>
</tr>
<tr>
<td>W₁(Cu)</td>
<td>Top copper pad width</td>
</tr>
<tr>
<td>W₂(Cu)</td>
<td>Bottom copper pad width</td>
</tr>
<tr>
<td>W₁(PI)</td>
<td>Top polyimide opening</td>
</tr>
<tr>
<td>W₂(PI)</td>
<td>Bottom polyimide opening</td>
</tr>
<tr>
<td>W(uB)</td>
<td>Micro-bump UBM width</td>
</tr>
<tr>
<td>W(B)</td>
<td>Bump UBM width</td>
</tr>
<tr>
<td>P₁</td>
<td>Top RDL pitch</td>
</tr>
<tr>
<td>P₂</td>
<td>Bottom wiring pitch</td>
</tr>
</tbody>
</table>

PROCESS FLOW

The frontend fabrication process is shown in Figure 2. A dual Damascene process is used to simultaneously define high density RDL and filled TSV:

a) 2 µm thick insulation layer is deposited by Chemical Vapor Deposition (CVD) of SiH₄ based silicon oxide at 400 °C, patterned and etched to define the copper pads (W₁=40 µm).

b) Via is patterned (W₂=20 µm) and etched slightly deeper than 100 µm target to allow room for backside tapping.

c) 1.5 µm Tetraethyl Orthosilicate (TEOS) liner isolates silicon sidewalls from the consequent metallization. This layer adds the total insulation layer at the front side to 2.5 µm. Conformality of coating is critical to subsequent electrical performance. TEOS films applied by plasma enhanced CVD provide excellent coverage and good stress and break down voltage (V_{BD}). Physical Vapor Deposition (PVD) of tantalum (Ta) and copper (Cu) defines diffusion barrier and seed layers, respectively. A 0.2 µm thick Ta was chosen to provide continuous and thick enough barrier at the via sharp corners and eliminate copper diffusion during thermal cycling.

d) TSV is filled by Electro Chemical Deposition (ECD), followed by Chemical Mechanical Polishing (CMP) to remove overburden on wafer topside and create the copper pads by Damascene process. Good fill and polish uniformity is needed for both steps.

e) Finally, polyimide passivation is applied, patterned and cured for solder masking.

Figure 2. Frontend process flow
Prior to backend process, wafer receives Electroless Nickel Palladium Immersion Gold (ENEPIG). Palladium acts as an additional barrier layer to further reduce copper diffusion to surface, thus ensuring good solderability. Palladium completely dissolves into solder, exposing an oxide-free nickel surface, allowing reliable formation of Ni/Sn intermetallic. Moreover, presence of Palladium eliminates grain boundary corrosion of nickel surface by immersion gold.

The target for via DRIE (100 µm) is:
- Non-uniformity < 2%
- Slightly tapered
- No or small necking, smooth sidewall

The target for liner CVD and barrier/seed PVD is:
- Liner: $V_{BD} > 50V$ for low power applications
- Continuous Barrier and seed

The target for copper ECD is:
- No voids/seems
- Good uniformity < 5%
- Minimize overburden to mitigate CMP risk
- Minimize dishing and erosion

The backend fabrication process is shown in Figure 3:

a) Wafer is flipped, temporary bond material is applied by spin coating or lamination [5, 6], and wafer is bonded to a carrier.

b) Grind backside to a distance close to TSV (to avoid copper contamination of silicon), followed by dry or wet etch to reveal via ($H > 0 \mu m$). Revealed alignment features are used for lithography steps.

c) Low-temperature CVD oxide or nitride passivation, this step should not violate the thermal budget associated with the bond material.

d) Backside “touch polish” to knock oxide off the bottoms of revealed via and expose metal. Alternatively, the insulation layer can be patterned and etched from the bottom of TSV.

e) Titanium and copper seed deposition, thick resist lithography and plate-through resist.

f) Strip resist and seed, polyimide patterning.

g) UBM (Ti/Ni/Cu) deposition by ECD, thick photoresist (PR) lithography and thick solder plating.

h) Strip resist and UBM, de-bond carrier wafer onto dicing tape, reflow solder.

In order to maintain a balanced structure and reduce chip warpage after de-bond, it is better to maintain similar overall stress for the top and bottom dielectric and passivation layers.

Figure 3. Backend process flow
**FABRICATION RESULTS**

Having fully defined the test vehicle and process flow in the previous sections, we built the interposer. Figure 4 shows cross section Scanning Electron Microscope (SEM) micrograph of TSVs after DRIE optimization. The etch recipe was optimized individually to obtain best roughness at the bottom of via and minimize necking at the top (below 0.5 μm). The etch profile is made slightly tapered profile (2°); via top is 0.6 μm wider than via bottom to facilitate good PVD coverage. Post-etch vapor-HF clean further removes the etch residues, and improves the roughness. After few iterations of DRIE, liner, barrier and seed coatings, the parameters of each module was optimized.

1.5 μm TEOS liner was chosen to satisfy the $V_{BD}$ requirement and the as-deposited stress was measured to be -160 MPa, which may be reduced by further thermal processes. Barrier and seed layer thicknesses were optimized to achieve enough coverage and low leakage, resulting in 0.2 μm and 2 μm, respectively. To minimize copper glomeration at the bottom of via, substrate temperature was kept low. Figure 5 shows cross section SEM micrograph of TSV bottom corner after liner, barrier and seed deposition. An acceptable barrier coverage and seed grain is obtained.

![Figure 4](image1.png)

**Figure 4.** Cross section SEM view of etched TSV: a) 500x, b) 5,500x showing smooth bottom sidewalls

![Figure 5](image2.png)

**Figure 5.** Cross section SEM view at 100,000x of TSV bottom after liner, barrier, and seed deposition confirms continuous barrier layer.

The 200 mm wafers were blanket plated to ~15 μm to fill the 20 μm wide TSVs. The current density and chemistry was optimized to improve copper thickness uniformity and eliminate void formation at the bottom of via, and minimize the overburden. As shown in X-ray micrograph of Figure 6, no visible void can be observed at the bottom of TSV’s.

![Figure 6](image3.png)

**Figure 6.** Tilted X-ray micrograph of the copper filled TSV shows void-free filling
Figure 7 shows cross section SEM view of TSVs after filling, proving fine grain TSV fill and small overburden. As shown in Figure 7.b the small necking caused by DRIE process has no effect on the fill process. A short 30 min anneal at 150 °C forming gas is used to minimize copper stress and pumping effect. Wafers were subsequently polished to remove overburden. The thickness standard deviation across 200 mm diameter after polish was below 2.5 µm.

The substrates were then bonded to carrier using 14 µm thick HT10.10 Brewer science material, and grinding was done with ±1 µm total thickness variation. Backside reveal process was done by silicon wet etch. KOH was used to remove silicon, selective to TEOS liner. The post-etch roughness was measured to be +/-0.3 µm. This roughness could likely get better with a polished surface, to begin with. Figure 8 depicts the TSV top-down view after reveal and CMP.

Figure 8. Microscope view of the revealed TSVs

In order to evaluate what oxide passivation conditions the bond material can survive, different thickness CVD oxide films were deposited at 150 °C, 200 °C, 220 °C and 250 °C on backside. The bond material survived all the process conditions without visible delamination. Figure 9 shows measured film stress of the 250 °C oxide for different thicknesses. The 1 µm oxide appears to have around -60 MPa of compressive stress, which is close to the combined stress of the oxide layers deposited on the front side.

Figure 9. Film stress measurement on the CVD oxide deposited at 250C for various thicknesses
Electrical properties of the TEOS liner and oxide passivation films were measured using mercury probe, as shown in Figure 10. Voltage was swept in 5 V steps to reach a threshold current of $5 \times 10^{-6}$ A. Breakdown voltage was measured by sweeping the voltage with a rate of 2 V/s, when the current reached $7 \times 10^{-7}$ A, the voltage was recorded as $V_{BD}$. The $V_{BD}$ was measured to be 507 V for TEOS and 552 V for the 250 °C SiH$_4$ based oxide films.

![Image](image1.png)

**Figure 10.** I-V curve and $V_{BD}$ measurement using Hg probe: a) TEOS liner, b) 250 °C oxide

Backside copper plating was demonstrated by plating 3 µm copper above the oxide passivation layer. As shown in tilted SEM view of Figure 11, acceptable grain size and uniformity (3 µm edge, 2.7 µm center) was obtained above rough surface of oxide. The thickness uniformity is not as critical as topside, since no polish is to be done at the backside. Surface has to be smooth enough to facilitate coarse lithography step needed to define bump openings.

![Image](image2.png)

**Figure 11.** Tilted SEM view of the plated copper pad

The de-bond process was done using Suss DB12S platform. The thermal slide process is shown in Figure 12. The substrate is secured using vacuum station, then HT10.10 Waferbond$^\text{TM}$ material is slowly heated above Tg, and finally the carrier wafer goes under twist and slide in three different stages to eventually de-bond the substrate. Figure 13 shows de-bond time vs. shear force curve for two pair of wafers in the de-bonder. The thin substrate was cleaned on the chuck and mounted on dicing tape. A dozen wafers were de-bonded using Waferbond$^\text{TM}$ and room temperature Zonebond$^\text{TM}$ materials [5].

![Image](image3.png)

**Figure 12.** Thermal slide process performed at Suss

**Figure 13.** Force-time curve for Suss de-bonder
About half of wafers were successfully de-bonded, as shown in Figure 14, and no cracks or chips were observed at the edge or near stress concentration points such as the notch.

For some wafers, the stress accumulated during thin film deposition, grinding, reveal, or plating resulted in edge cracks, which could later on grow during shipping. The crack propagation was observed only in the thinned wafers at points where edge chipping was present from thinning process, or at the bond voids sites due to de-bond thermal and shear stress. The bond voids, are believed to a result of vapor formation in the bond interface during backside passivation process, or other thermal processes, in the locations were bond is weak, or generated in random locations.

The Zonebond™ process, based on room temperature slide resulted in better yield compared to the thermal slide process.

**CONCLUSION**

In conclusion, we have provided a detailed demonstration of a model flow for Interposer fabrication. The challenges and issues related to each step have been highlighted and discussed. Although significant process optimization would be necessary to bring this design in to full production, it is our belief that the basic flow is consistent with a high volume manufacturing process. However, wide spread adoption of this technology is not only dependent on the technical feasibility but on the cost of manufacturing.

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