Cost-Minimized Double Die DRAM Packaging for Ultra-High Performance DDR3 and DDR4 Multi-Rank Server DIMMs

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Outline

- Key difficulties with current multi-die DRAM packages
- Newly developed structure
- Comparison of manufacturing process flows
- Device-level measured results
- DIMM PCB Design Comparison
- DIMM in system measured results
- Conclusion
Key Difficulties with Dual Die DRAM Package Structures

Opposing-Face DDP

- Dominated by Gold Cost
- Asymmetric signal and power delivery
- Thermal
- Thickness
- Cost

Face-Up DDP with RDL

- Dominated by RDL Cost
- Power and Signal Delivery via RDL
- Thermal
- Thickness
- Cost
PCB Layout difficulties with standard DDPs

Must interconnect same-named bussed signal to corresponding leads using “shoelace pattern”

Breakout pattern:
- Long stubs
- Mismatched stub length
- Signal integrity challenges at high frequency
Why do we have the long stubs in the breakout?

- Package evolution / legacy is the best answer

- Mass-Market DRAM have always had laterally displaced Address/Command signals

- Never created much of a timing issue until >1600MT/s operation became the target
Newly Developed Package: Invensas Dual Face Down: DFD™

Symmetric performance: similar to Single Die Package
Best thermals
Thinnest structure (no topside wire loops)
Lowest manufacturing cost
Invensas DFD: XRAY 2D CT Scan

Invensas Dual Face Down package: High Resolution Computerized Tomography – 2D Slices

XYZSlice; z height showing bond wires

XYZSlice; z height showing substrate routing
Invensas DFD: XRAY 3D CT Scan
### DFD Solves the C/A Stub issue elegantly

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### Description

- **C/A signals in dead center of package in the traditional “No Man’s Land”**
- **C/A region has simple breakout**
- **C/A Bus Signal ordering matches DDR3 register perfectly**
- **DQs and DQS signals close to package edge**
- **Most other signals only need simple through-hole connections to backside components**
- **Additional signals will be added to support DDR4**
Simplified Breakout Using DFD

Invensas DFD

Standard BGA
Electrical View: Standard BGA Package Breakout Stubs

Bussed Signals (multiple routing layers)

Cross-tied “Shoelace Pattern”

6-7mm
C/A Bus: Stub Issue

DDR3 1-to-4 C/A: Fly-by (Stub Length)

800Mbps (DQ信号1600Mbps)

Driver
DDR3 1.5V
DQ 340ohm Buffer

0.7mm

L1

L2

30mm

L3

40mm

20~70 Ohm

L1

L2

18mm

L3

30mm

L1

L2

18.0mm

L3

12mm

L1

L2

2mm

L3

L1

L2

Stub

L3

Stub

Short

Long

Fly-byトポロジーを選択してもスタブ長が長いとSIは維持出来ない。
A/Clk Simulation at DDR3-2133: 16% more margin at 75% faster operation

**DFD @ 2133**
- Window = 798 ps
- Ideal tCK = 938 ps
- 85% of a tCK

**JEDEC r/c D @ 1333**
- Window = 1093 ps
- Ideal tCK = 1500 ps
- 73% of a tCK
Electrical Considerations: Reference Planes for signals

All C/A signals referenced to Vdd in JEDEC DIMM Specs

DFD references C/A signals to Vdd in package providing consistent image current path: controller to memory die

DFD also references all non C/A signals to Vss for consistent image current path: controller to memory die
Forced Air Convection Heat Transfer Advantage

<table>
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<tr>
<th>Configuration</th>
<th>DFD (°C/W)</th>
<th>DDP (°C/W)</th>
<th>Delta from DDP</th>
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<td>( \theta_{ja} ) still air</td>
<td>36.6</td>
<td>48.7</td>
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<td>( \theta_{ja} @ 1m/s )</td>
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<td>( \theta_{ja} @ 3m/s )</td>
<td>22.6</td>
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<td>-25%</td>
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~25% lower \( \theta_{ja} \) for DFD vs. conventional DDP package
Manufacturing cost: process flows
Line flow example: DFD die attach and wirebond

Two Machine Insertions: die attach and wirebond all die for a dual die package
Line flow example: Opposing Face DDP die attach/wirebond

- DRAMs
- DRAMs (inverted in cassette)

1. Substrate strips
2. Die Pick/Place/Attach Machine
3. Wirebond Machine
4. Invert strip before 2nd wirebond operation
5. Wirebond Machine
6. Top die wirebond
7. Bottom die wirebond

Three Machine Insertions for die attach and wirebond
Line flow example: RDL DDP die attach/wirebond

Four Machine Insertions for die attach and wirebond

2nd Pass for 2nd Die
Wafer/Die Speed binning statistics

Die from a single wafer show tighter speed distribution vs multiple wafers/wafer lots

**DFD is only DDP that picks all die from same wafer**
Cost Comparison

Manufacturing Cost

- RDL DDP: $0.83
- Opposing Face DDP: $0.42
- DFD: $0.34
- Single Die Package: $0.20
Sort Yield Advantage: Invensas DFD vs Conventional DDP

Bin splits of yielded goods improved significantly

Speed Bin Yield vs. Control
1000 unit sample size (95°C testing)

- 67% Improvement in 2133MT/s Yield vs Control using same wafer lot

Leg A bottom, Leg B top

Leg D (top die only w/o substrate routing for lower die: performance is therefore optimistic)
DIMM Design Example: Multi-Rank Buffered DIMM PCB
Comparison: DDP vs DFD (Breakout layer)

Layer 1: Breakout, Isolation Devices, Register, TSE SPD
Comparison: DDP vs DFD (Address/Command)

Layer 4: Post-Register Device Address, Command
Comparison: DDP vs DFD (Data/Data Strobes)

Layer 3: Data routing
Measured RDIMM Results
Overview of RDIMM Evaluation Vehicle

- Invensas developed an 8GByte Quadranks x72 ECC RDIMM using the DFD package technology (dual 1 Gbit die/package)
- Each module contains 72 die of 1Gbit capacity (x4 die organization)
- Standard RDIMM edge connector/module form factor
- Initial testing: full speed in-system with Memtest 86
- Additional at-speed probing of signals in-system with 12GHz DSA
Instrumented DIMM With Probes Solder-Attached

For full-speed in-system probing of DQ, DQS
In-System Test Setup

12GHz Digital Signal Analyzer
Read Eye Diagram (Quadrank RDIMMs, 2DPC @1600MT/s)
Symmetric Performance

(DQx, DQS from die in same package)
DFD Reads Same Package, Both Die

DQS (DIE0)
DQS (DIE1)
DQ (DIE1)
DQ (DIE0)
Running Windows: Two DIMMs/Channel at 1700MT/s

Mem Data rate: 1705.8MT/s

This presentation prepared on this machine running at this speed
Conclusion

- A performance-enhanced cost-reduced double die DRAM package was developed.
- The package features a streamlined manufacturing flow and is the lowest cost way to assemble a given number of DRAM die.
- The bailout is very easy to use on a DIMM PCB: simple routing with minimal length stubs contribute to enhanced electrical performance.
- Thermal characteristics are more than 25% better than standard DDP.
- Significant simplification of DIMM PCB routing demonstrated.
- A quadrank RDIMM was developed and measured; with 2DIMMs/Channel reliable operation beyond 1700MT/s was observed.
- This talk was prepared using the test machine using 8 pieces of 8Gbyte Quadrank DFD RDIMMs in 2DPC configuration at 1700MT/s.