Reliability of Cu Pillar on Substrate Interconnects in High Performance Flip Chip Packages

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Agenda

- Flip Chip Technology
- Cu Pillar on Die Interconnects
- Cu Pillar on Substrate Interconnects
- 150µm Flip Chip Reliability Test Vehicle
- Calibrations and Test Protocols
- Experimental Results
- Failure Analysis and Discussion
- Reliability of 125µm pitch µPILR interconnects
- Summary
Flip Chip Technology: Benefits and Challenges

- Improved electrical and thermal performance due to shorter electrical paths between the die and the substrate
- Better power ground distribution
- High packaging density and scalability
- To reduce cost and propagation delays, migration from ceramic to organic substrates continues at an expense of larger CTE mismatch
- Close physical coupling of the die to substrate exposes the components to stresses which arise in packages during assembly and operation due to CTE mismatch
- Challenges due to increasing power and interconnect density and shrinking pitch requirements, transition to Pb-free bumps, low-k and ELK dielectric usage and electro-migration
- Stress reduction is easier if the mechanical coupling between the die and the package is reduced without affecting its electrical performance
Cu Pillar on Die Interconnects

- Tall Cu pillar on die is flip chip joined to substrates with solder on die pads in high performance applications

Advantages
- Fine pitch adaptability
- Taller interconnects facilitates underfill flow during assembly process
- Enhanced electrical and thermal conductivity of Cu reduces bump resistance and Joule heating and improves heat dissipation
- Improved electro-migration performance due to lower current density at the critical Cu/Sn interface

Disadvantages
- Cost
- More stress on fragile low-k and ELK dielectrics in high performance wafers
- Limited wafer bumping fabs are qualified to plate tall Cu pillars on die
Pillar on Die or Pillar on Substrate

- Need to design the interconnect and via stack on the wafer and introduce stress buffers to protect the low-k/ELK dielectric from stress imposed by Cu pillars on die.
- Such comprehensive optimization may not always be available to fabless semiconductor companies. Decoupling the interaction between the Cu pillar and the low-k ILD by other means may be an attractive option.
- Given the still limited number of wafer bumping fabs that are qualified to plate tall copper pillars on wafers, the alternative of shifting the tall pillars substrates could help users of extreme flip chip packaging (fine pitch, fragile ILD, Pb-free bumps, large die).
- The benefits of Cu pillar on die can be achieved by transferring the stiff stand-off to the substrate. The substrate fabrication process already uses Cu plating in a less demanding environment than that needed for wafers.
- If the Cu pillars on substrates need to be 30 to 50μm tall as well as retain tight co-planarity to duplicate the pillars plated on wafers, then bumping by plating would have to be in the process time of around 30 minutes. This may impact line utilization in a typical substrate Fab.
- The need to further reduce costs by depositing Cu pillars on the substrate by methods other than a straightforward transfer of process-to-plate pillar bumps on wafers to substrate panels.
Tessera μPILR™ Flip Chip Solution

- Competitive cost solution with improved assembly & reliability robustness
- Simple adoption through the standard substrate supply chain
- μPILR is a robust, scalable and cost effective solution for fine pitch flip chip

High co-planarity: etched copper pillar array on substrate improves assembly yield by eliminating opens and shorts resulting from solder on pad or plated pillar variation.

Allows the use of solder on die pad instead of copper pillar on die, reducing damage to the ELK layers.

Achieves higher stand-off and height/width aspect ratio allowing good underfill flow, higher yield and improved reliability performance.
Electromigration

- Electromigration is the mass transportation of atoms driven by both atomic diffusion and charge carrier mobility.

\[
\vec{J}_{\text{migration}} = -D \left( \nabla C + \frac{cQ^*}{k_BT^2} \nabla T + \frac{cZ^*e}{k_BT} \nabla \varphi + \frac{c\Omega}{k_BT} \nabla \sigma_m \right)
\]

- Highly temperature dependent
- Secondary dependencies: concentration and current density
- Calculating EM lifetime using Black’s equation

\[
MTTF = A \times J^{-n} \times EXP \left( \frac{E_a}{K \times T} \right)
\]
150µm Flip Chip Test Vehicle

Test vehicle designed to represent a high-performance flip chip package.
## Key Dimensions of the Test Vehicle

<table>
<thead>
<tr>
<th>Features</th>
<th>Dimensions (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Size</td>
<td>40 x 40 x 2 (3.2 thickness w/ HS)</td>
</tr>
<tr>
<td>Die Size</td>
<td>20 x 18 x 0.75</td>
</tr>
<tr>
<td>Substrate Thickness</td>
<td>1.19</td>
</tr>
<tr>
<td>UBM</td>
<td>Ti/W (0.2µm) / Cu (12µm)</td>
</tr>
<tr>
<td>UBM Diameter</td>
<td>90µm</td>
</tr>
<tr>
<td>Bump Composition</td>
<td>SnAg2.5</td>
</tr>
<tr>
<td>Passivation Opening on die</td>
<td>65µm</td>
</tr>
<tr>
<td>Solder Mask Opening on Substrate</td>
<td>90µm</td>
</tr>
<tr>
<td>Flip Chip Bump Pitch</td>
<td>0.15 (signal) and 0.2 (pwr/gnd)</td>
</tr>
<tr>
<td>Ni Plating Thickness</td>
<td>3-4µm</td>
</tr>
<tr>
<td># of Flip Chip µPILR Bumps</td>
<td>10,121</td>
</tr>
<tr>
<td>Heat Spreader</td>
<td>1.2µm Cu HS with Indium TIM</td>
</tr>
</tbody>
</table>
Electromigration Daisy Chain

Key Features

- 2-pair daisy chain with 2 anode (e- from die to substrate) and 2 cathode bumps
- Passivation opening on die: Ø65µm
- Solder mask opening on substrate: Ø90µm
- EM test conditions
  - 3 current levels: 40x, 50x and 60x103 A/cm²
  - 3 temperature levels: 140°C, 150°C, 160°C
- Cu UBM thickness: 12µm;
- Solder composition: Sn Ag2.5
- EM DC flip chip bump pitch: 150µm
# Electromigration Test Conditions

<table>
<thead>
<tr>
<th>EM Test #</th>
<th>Current (Amp)</th>
<th>Current Density (x $10^3$A/cm$^2$)</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.33</td>
<td>40</td>
<td>150</td>
</tr>
<tr>
<td>2</td>
<td>1.99</td>
<td>60</td>
<td>150</td>
</tr>
<tr>
<td>3</td>
<td>1.66</td>
<td>50</td>
<td>150</td>
</tr>
<tr>
<td>4</td>
<td>1.66</td>
<td>50</td>
<td>160</td>
</tr>
<tr>
<td>5</td>
<td>1.66</td>
<td>50</td>
<td>140</td>
</tr>
</tbody>
</table>

Sample size of 16 packages in each test condition

Black's equation

$$MTTF = A \times J^{-n} \times EXP\left(\frac{E_a}{K \times T}\right)$$

$MTTF$ is the Mean Time To Failure, which is related to $E_a$ (activation energy), $T$ (temperature), and $K$ (Boltzmann constant). The equation above shows how the failure rate increases with the current density and temperature in a logarithmic scale.

![Graph showing the relationship between ln MTTF and 1/kT](diagram.png)
Pre-Test Calibrations

- Temperature Coefficient of Resistance (TCR) Calibrations
  - Daisy chain resistances measured at 22°C, 50°C, 75°C, 100°C, 125°C, 150°C and 160°C
  - 50mA current for 4-point probe measurements; Data averaged over ~10-15min

- Joule Heating Calibrations
  - Curve generated by measuring the resistances of daisy chain at 0.5A, 0.75A, 1A, 1.25A, 1.5A, and 1.6A current stressing at room temperature
  - Measured ΔR is converted using TCR to estimate ΔT due to Joule heating
In-situ Resistance Monitoring

- Failure Criterion: >10% initial resistance
- Initial period of slow-steady rise in resistance
- µPILR: Initial slow and steady rise in resistance is followed by an abrupt jump in resistance when the part fails
- SOP: Rate of initial rise in resistance is slightly higher; not all parts fail with an abrupt rise in the bump resistance
Inter-Metallic Compounds and Void Nucleation

- Package with $50 \times 10^3$ A/cm$^2$ at 160°C
- failed after 634hrs
EM Failure in SOP Interconnects

- SOP Package with $60 \times 10^3$ A/cm$^2$ at 150°C failed after 352 hrs
EM Failures

- 100% failures on die side
- EM induced failure with loss of contact
due to large voids and UBM depletion
- Cathode bumps in SOP packages have EM damage on substrate side unlike µPILR

60x10^3 A/cm^2 at 150°C after 804h

60x10^3 A/cm^2 at 150°C after 1015h
Failure is defined as bump resistance rise greater than 10% of initial resistance.

Primary failures on die side in anode bumps with e- moving from die to substrate.

SOP bumps have substantial EM damage on cathode bumps (unlike µPILR).
## Statistical Analysis: 150µm Flip Chip

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test - 1 1.99A at 150°C</th>
<th>Test - 2 1.66A at 160°C</th>
<th>Test - 3 1.66A at 150°C</th>
<th>Test - 4 1.33A at 150°C</th>
<th>Test - 5 1.66A at 140°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>µPILR</td>
<td>SOP</td>
<td>µPILR</td>
<td>SOP</td>
<td>µPILR*</td>
</tr>
<tr>
<td>1st failure (hrs)</td>
<td>424</td>
<td>282</td>
<td>561</td>
<td>135</td>
<td>616</td>
</tr>
<tr>
<td>t_{63} life (η)</td>
<td>1404</td>
<td>706</td>
<td>1040</td>
<td>959</td>
<td>2669</td>
</tr>
<tr>
<td>t_{50} life (MTTF)</td>
<td>1223</td>
<td>624</td>
<td>954</td>
<td>821</td>
<td>2189</td>
</tr>
<tr>
<td>β</td>
<td>2.65</td>
<td>2.96</td>
<td>4.22</td>
<td>2.37</td>
<td>1.85</td>
</tr>
</tbody>
</table>

* Tests ongoing

### Test Conditions

<table>
<thead>
<tr>
<th>Test Condition</th>
<th>No of test hrs completed</th>
<th>Failures µPILR</th>
<th>Failures SOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test - 3</td>
<td>2250+</td>
<td>8</td>
<td>Completed</td>
</tr>
<tr>
<td>1.66A at 150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test - 4</td>
<td>2600+</td>
<td>7</td>
<td>11</td>
</tr>
<tr>
<td>1.33A at 150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test - 5</td>
<td>4075+</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>1.66A at 140°C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- EM lifetime is larger for the µPILR interconnect
Electromigration Discussion

- Reduction in bump resistance due to unique shape of µPILR
- Thick IMC accumulation around µPILR
- Reduction in diffusion gradient with µPILR on substrate
Temperature Cycle Test Results: µPILR vs. Cu-Pillar

- µPILR: 1st failure >2000 cycles
- Cu Pillar on Die: 1st failure at 1500 cycles
- MTTF µPILR >3000 cycles (1% Failures after ~1550 cycles)
- MTTF Cu Pillar on Die <2700 cycles (1% Failures after ~1000 cycles)
- µPILR significantly outperforms copper pillar on die interconnects in temperature cycling
Failure Mechanism During Temperature Cycling

Solder Fatigue failure in μPILR after 2250 cycles

Low-k failure in SOP packages after 1500 cycles

Die Crack
Reliability of 125µm µPILR Flip Chip

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Condition</th>
<th>Current Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL: Level3</td>
<td>125°C for 24hrs; 30°C/60%RH for 192 hrs, 3X Pb-free reflow</td>
<td>No failures after 192hrs</td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>150°C, 1000 hrs</td>
<td>No failures after 1000hrs</td>
</tr>
<tr>
<td>Unbiased Autoclave</td>
<td>121°C/100%RH/2atm for 168hrs</td>
<td>No failures after 168hrs</td>
</tr>
<tr>
<td>Temperature Cycling</td>
<td>-55°C to 125°C, 1000 cycles</td>
<td>No failures after 1250cyc</td>
</tr>
<tr>
<td>(Package Level)</td>
<td></td>
<td>(Test ongoing)</td>
</tr>
<tr>
<td>Temperature Cycling</td>
<td>-40°C to 125°C, 1000 cycles</td>
<td>No failures after 1250cyc.</td>
</tr>
<tr>
<td>(Board Level)</td>
<td></td>
<td>(Test ongoing)</td>
</tr>
<tr>
<td>Drop Testing</td>
<td>&gt;30drops, 1500Gs, 0.5mSec of half sine pulse</td>
<td>Test planned shortly</td>
</tr>
</tbody>
</table>

- **125µm pitch µPILR interconnect qualification for wireless applications**
Conclusion

- Reliability performance of fine pitch Pb-free μPILR interconnects and conventional thin Cu-UBM SOP interconnects in flip chip were investigated.
- Electromigration failures due to UBM depletion and excessive voiding on die-side in anode bumps; No damage to Cu-pillar on substrate irrespective of current direction; however substantial EM damage on substrate side to cathode bumps in SOP packages.
- Reduction in bump resistance compared to SOP with identical stand-off height; reduction in concentration gradient due to shorter Cu-to-Cu distance.
- Cu pillar on substrate interconnect demonstrates a large electromigration lifetime improvement over SOP structures.
- μPILR significantly outperforms copper pillar on die interconnects in temperature cycling.
- Cu pillar on substrate interconnect is better for high performance low-k/ELK applications.
- Demonstrated reliability performance of 125um pitch uPILR flip chip interconnects for wireless applications.