Direct Bond Interconnect (DBI®) Technology as an Alternative to Thermal Compression Bonding

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Outline

- Introduction
- Test Vehicle Design & Fabrication
- Bonding Process Development and Qualification
- D2W Hybrid Bonding Results
- Summary
- Acknowledgements
### 3D Stacked DRAM Technology Trends Enabled by TCB

<table>
<thead>
<tr>
<th>Applications</th>
<th>DDR4 3DS</th>
<th>HBM</th>
<th>HMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density (GB)</td>
<td>2</td>
<td>2-4</td>
<td>2-4</td>
</tr>
<tr>
<td>DRAM Die(s)/Logic Die (s)</td>
<td>4/0</td>
<td>4-8/1</td>
<td>4/1</td>
</tr>
<tr>
<td># of TSVs/die</td>
<td>136</td>
<td>2472</td>
<td>Est &gt; 2000</td>
</tr>
<tr>
<td>TSV pitch (um)</td>
<td>125</td>
<td>40</td>
<td>Est 40</td>
</tr>
<tr>
<td>Max Bandwidth (GBps)</td>
<td>25.6</td>
<td>256</td>
<td>240</td>
</tr>
<tr>
<td>Testing</td>
<td>Standard</td>
<td>Low speed, 1024 bits</td>
<td>High speed, 64 bits</td>
</tr>
</tbody>
</table>
TCB Challenges and Potential Solution

- **TCB challenges:**
  - Process control and low yield in bonding
  - Low throughput
  - Thermal performance in multi–die memory stacks
  - Stress over large die/packages (ΔCTE) and warpage
  - Scaling limitations (40 µm today)

- **Solution: Low temp hybrid bonding**
  - Simpler process (no solder or underfill)
  - Room temp bond (throughput)
  - Die stack has properties of a single die
  - Improved thermal performance
  - Architectural flexibility “If you can print it; you can connect it…“

![Graph showing assembly window versus pitch](image)
W2W Dielectric Bonding and Low Temperature Hybrid Bonding Process
Simplification of 3D Stacking

- Thermal compression bonding (TCB) at reflow (240°C)
- High warpage, leads to yield loss
- Underfill challenges (flow, standoff, pitch)
- Solder interconnect, pitch limitations (40µm)

- Low temp bonding (25°C)
- Batch anneal temp. (~150–300°C)
- Low warpage in final product improves yield
- Scalable to ultra-fine pitch (down to 1 µm)

HBM 4-high stack with TCB
With hybrid bonding
Bond Pad Structure Simplification

- UBM,
- Ti, Cu, Ni (sometimes)
- SAC

µbump

Hybrid bonding pad

- Cu Routing of direct bond interconnect; BEOL
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Test Vehicle Design Features

- Single side die (phase 1)
- 4 die stack without TSVs (phase 2)
- 4 die stack with TSVs (phase 3)
- Grid bond pads to tolerate 10µm misalignment (patent pending*)
- Uniform grid array on bonding surface
- Daisy chains throughout stack (for phase 3)

* US patent application number: 62/269,412
Silicon Supply Chain Development

- Developed multiple partners with critical capabilities
  - CMP
  - TSVs
- Developed in-house AFM capability and expertise for bonding surface characterization
- Fabricated Daisy Chain wafers for D2W stacking
Bonding Surface Characterization

- In house AFM capability for 300mm wafer
- Color enhanced AFM image of a bonding surface with Cu recessed from oxide
Test Vehicle Fabrication Process

Host wafer and single sided daisy chain die wafer

Double sided daisy chain die wafer
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Bonding Process Challenges

Thin wafer handling and dicing protocol

Cleaning recipe

Plasma activation recipe

Bonding recipe, Bond energy

CSAM for bonding void

Die Wafer

Dicing

Clean

Activation

Host Wafer

Clean

Activation

Bond

Anneal 150C, 15min

CSAM
Bonding Process Development–1: W2W Bonding

- Use off-the-shelf thermal oxide wafers for
  - Cleaning recipe
  - Activation recipe
  - Bond energy measurement

Diagram:
- TOX Wafer
- Cleaning recipe
- Clean
- Activation
- Bond energy
- Bond
- Anneal 150C, 15min
- CSAM
Bonding Process Development–2: D2W Bonding

- Thin and dice off-the-shelf thermal oxide wafers for
  - Thin wafer handling & dicing protocol
  - Bonding recipe
  - CSAM protocol for bonding void characterization
Cleaning

Die front side particle contamination from saw dicing

Die back side tape residue

Die surface after wet clean
Bond Energy Measurement

BE (mJ/m²) = (3 × h² × E × t³)/32 × L⁴

BE: Bond Energy
h: Razor blade thickness, in mm
E: Young’s Modulus of silicon, in Pa
t: Wafer thickness, in mm
L: Observed crack length, in mm

Target Value: BE > 2000mJ/m² after full anneal
Plasma Activation DOE

- Bond Energy after 150°C, 15 min anneal
  - >2000 mJ/m² after short anneal
  - Wide process window for 1500 mJ/m² target

<table>
<thead>
<tr>
<th>Parameter 1</th>
<th>Parameter 2</th>
<th>Parameter 3</th>
<th>Bond Energy (mJ/m²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>1747</td>
</tr>
<tr>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>2032</td>
</tr>
<tr>
<td>Low</td>
<td>Middle</td>
<td>Low</td>
<td>1883</td>
</tr>
<tr>
<td>Low</td>
<td>Middle</td>
<td>High</td>
<td>2032</td>
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<tr>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>1883</td>
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<tr>
<td>Low</td>
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<td>High</td>
<td>1747</td>
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<td>High</td>
<td>High</td>
<td>High</td>
<td>2032</td>
</tr>
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</table>
CSAM of Oxide Bonding Interface

- Progression of bonding void reduction

Early stage, large particles on surface
- Large void

Small particles on surface
- Small voids

Clean surface
- No voids
Bonding Process

- Bonding using in-house TCB bonder and P&P Tool
- Compatible with high throughput P&P tool
- Ambient condition, very low force
- No underfill, no adhesive
- <1s bonding time (vs 8–30s for TCB)
- Batch anneal after bonding, no fixture needed
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E-test Results

- Measurement after 300°C anneal
- 8" host wafer
- 73% yield on 1st wafer
- 96% yield on most recent build
Cross-Section Analysis

- Good bonding interface
- Very solid Cu–Cu joints
- No void
- No intermetallic layer
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D2W hybrid bonding has been demonstrated using daisy chain test vehicles that mimic HBM die size and interconnect pitch.

E–test yield of 96% has been achieved.

Compared to µbump TCB, D2W hybrid bonding process is much simpler, very low force, ambient bonding and as fast as flip chip bonding.

A wet cleaning process leads to virtually void free bonding.

Plasma activation process window is very wide and well suited for HVM.
Aknowledgement

- Novati Technologies
  - Daisy chain wafer fabrication
- Fraunhofer IZM ASSID
  - Plasma activation DOE
Thank You!

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