Invensas™ Multi-die DRAM Packaging Overview

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Overview:

Invensas has developed two new multi-die DRAM package technology families. Both are designed to solve specific system integration problems of growing importance in the industry.

The first offering, called the Dual Face Down (“DFD”) package is targeted at the high density and high performance DIMM markets. Designed to optimize PCB layout, high speed signal integrity and thermal performance, these dual die packages are made using standard Face-Down process flows and existing wirebond BGA assembly and test infrastructure with a streamlined manufacturing process flow for the lowest cost.

The second offering, called the “DIMM-in-a-PACKAGE” memory device, accommodates four devices in a single component (Quad Face Down, “QFD”), and is specifically targeted to the new ultra-slim form-factor notebook PCs such as Ultrabooks™ and tablets. Using a common ballout scheme that is optimized for efficient PCB layouts on low-cost through-board via PCB technology (“Type 3 PCB”), a common ballout accommodates DDR3x, DDR4x and LPDDR3 devices. When used with the appropriate CPU, PCB-level co-support of DDR3x and LPDDR3 is offered for Ultrabooks using single or double sided assemblies on Type 3 PCBs.

Common to both product families is the use of existing high-volume wirebond-based face-down window-BGA DRAM assembly infrastructure. No new capital equipment is required for the assembly operations. No Redistribution Layer (“RDL”) is required and using common wirebond BGA assembly the unique structures offer single-pass line assembly.

Both families offer very thin stackups with no height increase arising from the use of spacer die. The face-down die orientation minimizes wirebond length and avoids the need for thick encapsulation above the die versus face-up wirebonding. The result is a dual-die package (“DDP”) that is 1 mm thick or quad-die package (“QDP”) 1.2 mm thick. The thin profile coupled with the die not being stacked directly atop one another offers significant thermal advantages further augmented by a larger number of signal connections to the PCB. The reduction in Z height above PCB increases the air gap between DIMMs to assist in cooling airflow.

DFD details:

Unlike traditional stacked-die DDPs, the DFD features separated DQ signals making it ideal for bandwidth intensive applications. Built using a variant of the high-volume window-BGA face-down package, a live die and a spacer die are mounted facing a substrate containing two bonding windows. The second memory die is stacked above the second bonding window in a shingle-like configuration (Figure 1). The result is a 104 ball 11.5 x 11.5 x 1 mm package with 0.8 x 0.8 mm ball pitch. Detailed manufacturing cost models show that the DFD costs 1.8x the cost of a single die package (“SDP”), meaning the cost per die is actually lower than for an SDP.
Figure 1: DFD structure

One of the key design features of the DFD is the placement of the Command/Address (“CA”) signals in the center of the package. This solves the well-known cross-tie stub problem associated with standard single, double and quad die packages used on double-sided assemblies by decreasing the distance the cross tie stubs must be routed in the breakout region (Figure 2). Another feature of the DFD is the ability to route the CA global bus in a single layer in a standard DIMM PCB process (Figure 3). This avoids layer to layer timing skew that limits operating frequency. Finally the DQ signals are located at one end of the package to permit very short interconnection with other devices on the DIMM to enable the highest operating frequency.

Figure 2: breakout regions compared: DFD vs. single / standard BGA package

High performance quadrank RDIMMs and HyperCloud™ DIMMs have been demonstrated using the DFD technology. The quadrank RDIMMs have been shown to operate reliably at 1600MT/s DDR3 rates using two quadrank RDIMMs/channel. Single quadrank DFD-based RDIMMs have been demonstrated at 1866MT/s.

The DFD is not limited to the mission critical needs of the modern datacenter. The compact and thin dual-die structure provides the only cost-effective way to make a 2mm thick single-sided 8-die SODIMM. Using dual x8 devices a single-rank structure can be implemented using only 4 packages mounted on a single side (Figure 4). The small footprint required by the memory packages allows cost-effective 0402 passives to be used. Using both sides a 16-die 3mm thick SODIMM can be constructed using 0402 passives. The emerging MicroDIMM and other DIMM standards can benefit from the use of the DFD in a similar manner.
DIMM-in-a-PACKAGE Technology:

The second key market focus area for Invensas has been the emerging Ultrabook and Tablet markets. These and other ultra-slim notebook and tablet devices have largely been turning to solder-down single-die packaged memory and expensive HDI build-up PCB technology (“Type 4 PCB”). The aggressive vertical dimensions simply do not accommodate SODIMMs in the slimmest form-factors.

The Invensas offering is called the DIMM-in-a-PACKAGE memory device. Offering the full functionality of an SODIMM, including an optional SPD/TSE in a single BGA, the device is configurable as a single x64 or a dual channel x32 memory system in a package. The package is a 407 ball BGA using 0.8 mm pitch and is 17.5 x 22.5 x 1.2 mm. A key feature of this technology is a common compatible ballout that supports DDR3x, DDR4x and LPDDR3 (Figure 5).
Manufacturing:

The packages using this common ballout can be constructed using a variety of methods including 4-die structures featuring face-down window BGA assembly methods. This leads to a very efficient manufacturing flow: all of the die are placed in a single operation. Next, all of the die are wirebonded in a single operation offering the same strips/hour assembly throughput on the same machinery as standard single-die packaging (Figure 6). This is the method used for building the high volume DDR3 and DDR4 versions of the DIMM-in-a-PACKAGE devices as well as the center bonded x16 LPDDR3 version. The x32 periphery-bonded LPDDR3 versions are assembled in a 2-die face-up wirebonded configuration featuring one pass die placement and one pass wirebonding as for the four die face down versions. Detailed cost models indicate the QFD assembly costs 3.8x the cost of an SDP to manufacture. Like for the DFD, on a per-die basis this is less than for an SDP.

Because of the common ballout the same test hardware can be used for testing DDR3, DDR4 and LPDDR3 versions of the device. This consolidation of test fixturing greatly reduces the capital investment otherwise needed to support these different DRAM technologies, each commanding or expecting to command significant market share in these slim and portable applications.

System OEM/ODM Advantages:

For the system OEM and ODM the benefits are numerous. A key design goal was efficient PCB layout using a standard low-cost Type 3 PCB. Additionally when using the second generation Ultrabook CPU that offers co-support of LPDDR3 and DDR3 a single low-cost Type 3 PCB can be designed supporting either type of memory as a BOM build-time option. This greatly reduces the cost of design and manufacturing by having a master design capable of spanning the SKU matrix by BOM options.

Using previous generation layout guidelines a 40% reduction in area was attained by migrating to a 12 layer Type 4 design made using single die packages to a low cost type 3 PCB using the DIMM-in-a-PACKAGE devices (Figure 7).

Key to the efficient PCB layout is the symmetric ball map developed. The ball map features two copies of the CA bus arranged in a mirror-image symmetry about the Y-axis. Each CA bus connects to half of the memories in the device. Depending on how wired in the system, each DIMM-in-a-PACKAGE memory device can be used as a single x64 or a dual x32 memory system. This offers many benefits for the Tablet market as well as embedded applications such as femtocells. The thin 1mm package with die spread out on the substrate is both thinner and has significantly better thermal characteristics versus stacked die QDPs. This is of great importance in these new ultra-thin portable devices.

The DIMM-in-a-PACKAGE is not limited solely to solder-down memory applications. Using board to board connectors a dual channel module can be constructed that is the same XY size as an SODIMM but sits no higher.
than 3.5mm above the lower PCB. Using double sided assembly a 16-die dual-rank dual-channel module can be constructed.

**Figure 6:** Manufacturing flow for Assembly of QFD

**Figure 7:** Invensas DIMM-in-a-PACKAGE device saves 40% of memory footprint using Type 3 PCB