

INVENSAS BVA POP FOR MOBILE COMPUTING:

100+ GB/s BVA PoP

The Bond Via Array™ (BVA™) Package-on-Package (PoP) technology offers the highest bandwidth packaging solution for mobile phones and tablets. With more than 1000 interconnects at 0.24 mm pitch, this product enables up to 512bit memory bus between the multi-core CPU/GPU processors and DDR3/DDR4/Wide IO memory within 14mm x 14mm package size. With 800 MHz memory devices, an unprecedented 100 GB/s bandwidth can be achieved between the processor and the memory packages. This performance is achieved through advanced packaging at low cost utilizing existing materials and infrastructure.

Key Benefits to OEM

Higher performance: Ultra-high IO (quad-channel+, up to 512bit wide) between the bottom logic package and the top memory package offers up to 100+ GB/s bandwidth.

PoP approach: Independently sourced, packaged, and tested logic and memory for high yield and supply chain flexibility

Memory compatibility: Utilizes current LPDDR2 and LPDDR3, while scalable to wide IO memory devices

High-level package reliability and low cost: Utilizes established assembly equipment, processes and materials

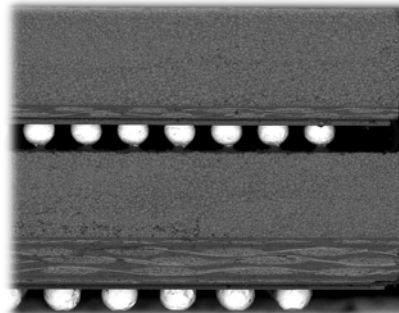
Key Benefits to IDM

Logic (bottom) package:

- Conventional flip-chip packaging of logic device on high-density substrate
- >1000 logic to memory interconnects in a standard 14 mm x 14 mm package
- Logic to memory interconnects formed through free-standing wires utilizing industry proven wire-bond equipment infrastructure
- Fully molded package for minimal warpage
- Industry standard LGA/BGA at the bottom

Memory (top) package:

- Conventional single or multi-chip CSP package
- Any type of memory including current LPDDR2, LPDDR3, and the future wide IO
- Package level multi-channel IO (up to 512x) by using one or more memory chips having wire-bond or flip-chip interconnects within package



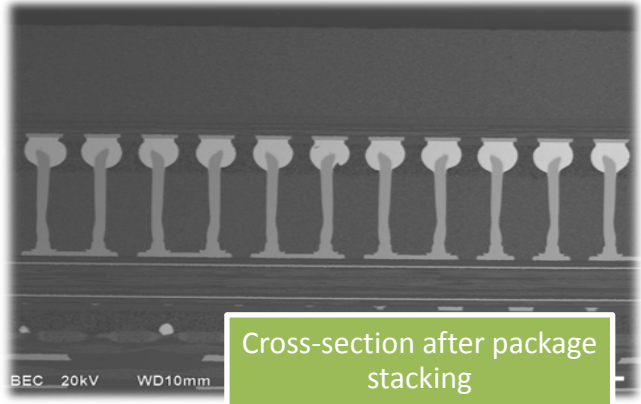
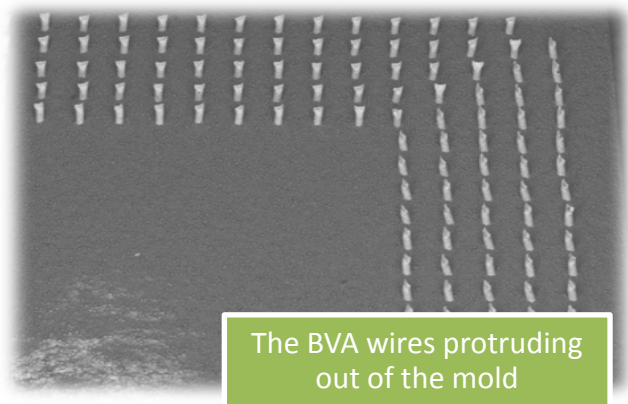
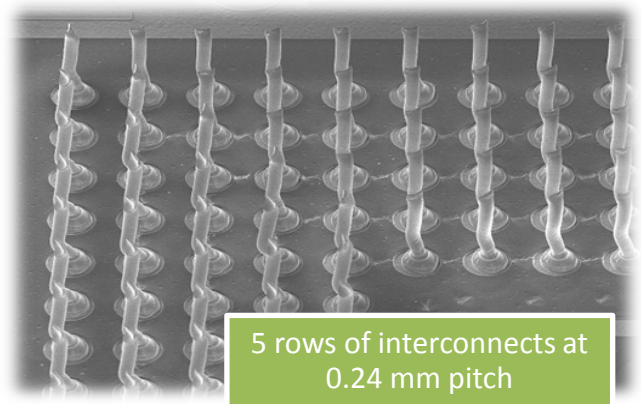
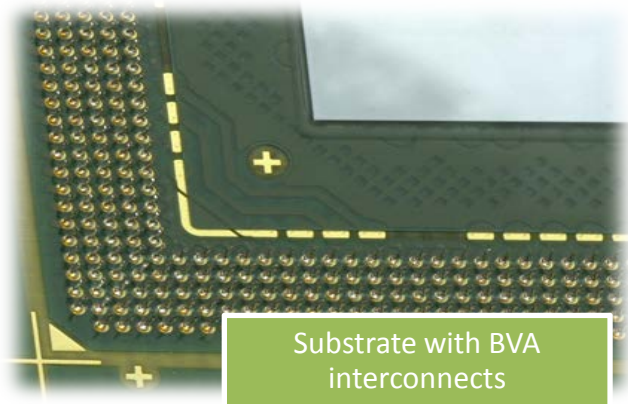
Key Benefits to System Assembler

Simple PCB Design and PoP Assembly

- Keeps all high IO memory-logic routing off the main board and within the PoP
- Conventional board assembly by placing the logic package on main board, placing memory package on top of logic package and single reflow pass for full board assembly

High performance computing at low power utilizing ultra-high IO bandwidth between local high capacity memory and multi-core logic (CPU/GPU)

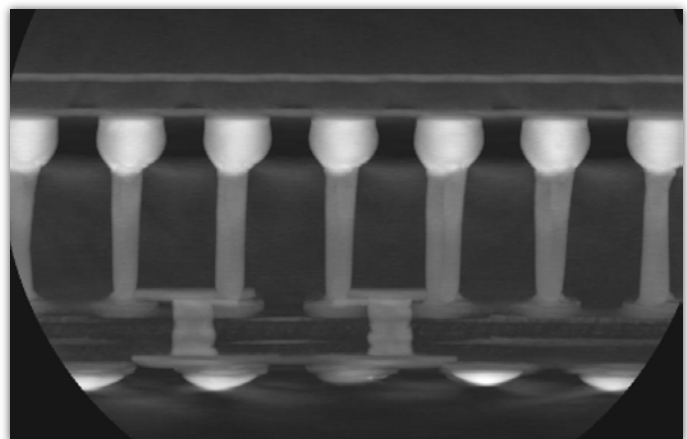
Bond Via Array (BVA) PoP Features



Fine pitch and high IO package manufacture using conventional equipment and materials

Reliability Test Results

Test	Standard	Test condition	Sample size	Status
Moisture sensitivity Level 3	IPC/JEDEC-J-STD-020C	125°C for 24hrs; 30°C/60%RH for 192 hrs, 3X Pb-free reflow	22 logic and 22 memory packages	Pass
High temperature storage	JESD22-A103D-condition B	150°C, 1000 hours	22 PoP off-board	Pass
Unbiased autoclave	JESD22-A102D-condition D	121°C/100%RH/2atm for 168 hours	22 PoP off-board	Pass
Drop test	JESD22-B111	>30 drops, 1500 G, 0.5 msec of half sine pulse	20 PoP on board with underfill	Pass (no failures till 128 drops)
Temperature cycling (board level)	JESD22-A104D Condition G	-40°C to 125°C, 1000 cycles	45 PoP on board with underfill	Pass



BVA PoP package passed all reliability tests by meeting or exceeding requirements.

Invensas offers BVA PoP design services. Contact info@invensas.com for more information.

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